CLAIMS

WHAT IS CLAIMED IS:

1. A memory control system comprising:

a processor for operating upon fetching a program through a system bus and stopping its own operation and outputting an internal power-down signal upon fetching a sleep command; and

a power-down control circuit for outputting, upon receiving said internal power-down signal, a control signal to put a volatile semiconductor memory connected to said system bus into a self refresh mode.

2. The memory control system according to claim 1, wherein

said program including said sleep command is stored in said volatile semiconductor memory.

3. The memory control system according to claim 1, comprising

a clock control circuit for receiving a clock disabling signal output from said power-down control circuit and stopping supplying a system clock signal, and wherein

said power-down control circuit outputs said clock disabling signal after said volatile semiconductor memory is put into said self refresh mode.

4. The memory control system according to claim 3, wherein

said clock control circuit is a phase-locked loop circuit for generating said system clock signal having a phase the same as a phase of an external clock signal.

5. The memory control system according to claim 1, wherein:

said power-down control circuit outputs an operation enabling signal to said processor after releasing said volatile semiconductor memory from said self refresh mode in response to a sleep release request; and

said processor starts fetching said program after receiving said operation enabling

signal.

6. The memory control system according to claim 5, comprising

a clock control circuit for receiving a clock enabling signal output from said power-down control circuit and starting supplying a system clock signal, and wherein

said power-down control circuit releases said volatile semiconductor memory from said self refresh mode after outputting said clock enabling signal.

7. The memory control system according to claim 6, wherein

said clock control circuit is a phase-locked loop circuit for generating said system clock signal having a phase the same as a phase of an external clock signal.

8. The memory control system according to claim 1, wherein:

said power-down control circuit includes a memory control circuit for directly controlling said volatile semiconductor memory, and a main control circuit for controlling said memory control circuit;

said main control circuit outputs a power-down request signal to said memory control circuit in response to said internal power-down signal; and

said memory control circuit outputs said control signal in response to said power-down request signal, and outputs a power-down acknowledge signal to said main control circuit in response to said volatile semiconductor memory being put into said self refresh mode.

10030530.010702